Office Action Summary	Application No.	Applicant(s)	
	10/618,284	BROOKES ET AL.	
	Examiner	Art Unit	
	SAIF A. ALHIJA	2128	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-16,18,19 and 24-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *1,5-16,18,19 and 24-37* is/are allowed.

6)☒ Claim(s) *38-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20090716*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 5-16, 18-19, and 24-49 have been presented for examination.

Claims 2-4, 17, and 20-23 have been cancelled.

Claim 38-49 are newly presented.

Response to Arguments

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4 June 2009 has been entered.

PRIOR ART ARGUMENTS

i) Following Examiners amendment for which authorization was provided by J. Matthew Zigmant, 44005 on 16 July 2009 claims 1, 5-16, 18-19, and 24-37 are allowable. However newly presented claims 38-49 are rejected. The Examiner requested Applicants representative to amend the claims in accordance with claims 1, 15, or 29 however no agreement was reached. The Examiner notes that an amendment was suggested for claim 38 however since the claim was not rendered allowable the Examiner respectfully requests that the amendment be submitted in the response to this office action.

ii) Newly presented claims 38-49 are rejected below.

EXAMINERS NOTE

iii) Examiner has cited particular columns and line numbers in the references applied to the claims for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

iv) The Examiner respectfully requests, in the event the Applicants choose to amend or add new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution.

v) Further, the Examiner respectfully encourages Applicants to direct the specificity of their response with regards to this office action to the broadest reasonable interpretation of the claims as presented. This will avoid issues that would delay prosecution such as limitations not explicitly presented in the claims, intended use statements that carry no patentable weight, mere allegations of patentability, and novelty that is not clearly expressed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 38-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kim et al. "Combined Data-Driven and Event-Driven Scheduling Technique for Fast Distributed Cosimulation", hereafter Kim** in view of **Ghosh et al. "A Hardware-Software Co-simulator for Embedded System Design and Debugging", hereafter Ghosh.**

Regarding Claim 38:

The reference discloses A method for simulating a system which comprises a software element and first and second hardware components, the software element being for execution on the second hardware component, and the first and second hardware components being operable to interact with one another, the method comprising:

receiving a variable synchronization parameter; ; **(Kim. Section III, paragraph 4, "In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.")**

simulating operation of the first hardware component in a first simulation; ; **(Kim. Figure 5, HW)**

simulating the software element and the second hardware component in a second simulation; and **(Kim. Figure 5, SW)**

running the second software simulation asynchronously with, and ahead of, the first software simulation, wherein the second software simulation advances at most by a number of processor clock cycles set in the variable synchronization parameter before the first software simulation advances by a clock cycle, **(Kim. Section III, paragraph 4, "In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.")**

Kim does not explicitly recite threads but rather recites tasks.

Ghosh further discloses separate processing threads within the host machine **(Ghosh, Page 157, top right, "The co-simulator is implemented as a multithreaded program to allow easy integration of stand alone simulators.")**

Kim and Ghosh are analogous art in Hardware Software CoSimulation.

It would have been obvious to one of ordinary skill in the art at the time of invention to analyze and validate as per **Ghosh** the simulation of **Kim** in order to determine if the resultant design is working correctly and further with respect to threads see citation of Ghosh Page 157 top right.

Regarding Claim 39:

The reference discloses method of claim 38, wherein the variable synchronization parameter limits a maximum number of processor clock periods of the second simulation per period of a reference clock of the host machine **(Kim. Section III, paragraph 4, "In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.")**

Regarding Claim 40:

The reference discloses The method of claim 38, wherein the first and second simulation run asynchronously. **(Kim. Page 673, left column, asynchronous clocks)**

Regarding Claim 41:

The reference discloses The method of claim 38, wherein a number of clock cycles of the first simulation and the second simulation are synchronized with a reference clock. **(Kim. Section III, paragraph 4, "In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.")**

Regarding Claim 42:

The reference discloses The method of claim 38 further comprising:

performing operations in the first simulation to set up an inter-process communications protocol connection therein; **(Kim. Abstract, "intersimulator communications")(Kim. Section VI-C, TCP/IP)**

Kim does not explicitly recite connecting a software debugger to the communications protocol connection; and

and controlling the first software simulation system from the software debugger using the interprocess communications protocol.

However Ghosh discloses connecting a software debugger to the second software simulation system; **(Ghosh. Abstract, "debugging software")**

and controlling the first software simulation system from the software debugger via the second software simulation system using the interprocess communications protocol. **(Ghosh. Abstract, "debugging software")**

It would have been obvious to one of ordinary skill in the art at the time of invention to debug as per **Ghosh** the simulation of **Kim** in order to determine if the resultant design is working correctly.

Regarding Claim 43:

The reference discloses The method of claim 38, wherein the second hardware component includes embedded processors. **(Kim. "embedded system design") (Ghosh. Section 2, "embedded processor")**

Regarding Claim 44:

The reference discloses A method for controlling a simulation of a system using a software debugger, wherein the system comprises a software element, and first and second hardware components, the software element being for execution on the second hardware component and the first and second hardware components being operable to interact with one another, the method comprising the steps of:

simulating the first hardware component in a first simulation; **(Kim. Figure 1 c, processor simulator B, ipsimulator C, and hardware simulator D)**

simulating the second hardware component in a second simulation; **(Kim. Figure 1 c, processor simulator B, ipsimulator C, and hardware simulator D)**

performing operations in the first simulation to set up an inter-process communications protocol connection; and **(Kim. Abstract, "intersimulator communications")**

Kim does not explicitly recite controlling the first software simulation system from the software debugger using the interprocess communications protocol.

However Ghosh discloses controlling the first software simulation system from the software debugger via the second software simulation system using the interprocess communications protocol. **(Ghosh. Abstract, "debugging software")**

It would have been obvious to one of ordinary skill in the art at the time of invention to debug as per **Ghosh** the simulation of **Kim** in order to determine if the resultant design is working correctly.

Regarding Claim 45:

The reference discloses The method of claim 44, further comprising the step of: connecting the software debugger to the inter-process communications protocol connection. **(Kim. Abstract, "intersimulator communications")(Ghosh. Abstract, "debugging software")**

Regarding Claim 46:

The reference discloses The method of claim 44, wherein the step of simulating the second hardware component comprises simulating a processor and one or more peripheral devices with which the one or more processors interact directly. **(Kim. "embedded system design") (Ghosh. Section 2, "embedded processor")**

Regarding Claim 47:

The reference discloses The method of claim 44, wherein the first simulation and the second simulation run asynchronously. **(Kim. Page 673, left column, asynchronous clocks)**

Regarding Claim 48:

The reference discloses The method of claim 44, wherein the first simulation and the second simulation are synchronized with a reference clock. **(Kim. Section III, paragraph 4, "In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.") (Kim Page 673, left column, asynchronous clocks)**

Regarding Claim 49:

The reference discloses The method of claim 44, wherein the second hardware component includes embedded processors. **(Kim. "embedded system design") (Ghosh. Section 2, "embedded processor")**

Allowable Subject Matter

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with J. Matthew Zigmant, 44005 on 16 July 2009.

The application has been amended as follows:

1) Please amend claim 1 as follows:

receiving a dynamically variable synchronization parameter wherein the dynamically variable synchronization parameter is dynamically variable while simulating the software element and the second hardware component in the second software simulation system;

running the second software simulation system asynchronously with, and ahead of, the first software simulation system, wherein the second software simulation system advances at most by a number of processor cycles set in the dynamically variable synchronization parameter before the first software simulation advances by a clock cycle, the dynamically variable synchronization parameter limiting a maximum number of processor clock periods of the second simulation per period of a reference clock of the host machine;

2) Please amend claim 15 as follows:

receiving a dynamically variable synchronization parameter wherein the dynamically variable synchronization parameter is dynamically variable while simulating the software element and the second hardware component in the second software simulation system;

running the second software simulation system asynchronously with, and ahead of, the first software simulation system, wherein the second software

simulation system advances at most by a number of processor cycles set in the dynamically variable synchronization parameter before the first software simulation advances by a clock cycle, the dynamically variable synchronization parameter limiting a maximum number of processor clock periods of the second simulation per period of a reference clock of the host machine;

3) Please amend claim 29 as follows:

wherein the reference clock parameter is dynamically variable and selectable while simulating the embedded input/output device within the simulation model in the second software simulation;

The following is an examiner's statement of reasons for allowance: claims 1, 5-16, 18-19, and 24-37 are considered allowable since when reading the claims in light of the specification, none of the references of record alone or in combination disclose or suggest the combination of limitations specified in the independent claims, specifically:

The recitation with respect to claim 1 of a dynamic variable synchronization parameter in combination with the second simulation running ahead of the first simulation and controlling the first simulation.

The recitation with respect to claim 15 of a dynamic variable synchronization parameter, in combination with the second simulation running ahead of the first and controlling the first simulation through the software debugger.

The recitation with respect to claim 29 of a dynamic variable synchronization parameter in combination with the interactive program, and polling aspects of the claim.

The claims are rendered statutory since the claimed methods require the use of a computer to implement the HDL simulation environment. See page 5, lines 7-30 of the specification of the instant application.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Claims 1, 5-16, 18-19, and 24-37 are allowable.

Claims 38-49 are rejected.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAIF A. ALHIJA whose telephone number is (571)272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128

SAA

July 16, 2009